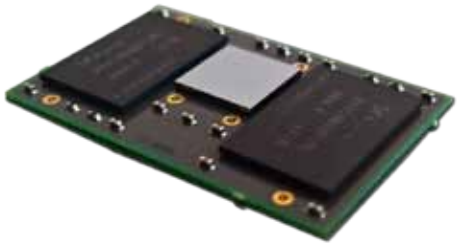
ASIC Development

Dream Chip Technologies offers the design of complete ASICs, including mass production delivery and supports customers on their own development projects with engineering teams or individuals.

Depending on the ASIC use-case the development focus is on: low power, low cost, high / low complexity or / and security.

Full Turnkey ASIC / SoC Delivery:

- small to high volumes
- silicon testing
- silicon packaging
- delivery through Dream Chip



Front end design:

- Cadence and Synopsys
- Power analysis: Cadence, Apachee
- Feedback control systems: Matlab / SimuLink models
- HDL Languages: Verilog and VHDL

Processor Experience:

- ARM
- Tensilica
- MIPS
- ARC / Virage
- Pico (32 bit risc)
- Customer custom processors

Physical design / backend:

- **Tools**
  - Synopsys tool chain
  - Cadence tool chain
  - Mentor Calibre
  - Apache Redhawk
  - Synopsys Primetime
- **Methodology**
  - synthesis and P&R
  - fully automated flow for deterministic results
  - automated log file checks
  - advanced scripting for timing closure
- **Primetime**
  - fully automated regression
  - reporting summary
  - automated feedback of sign-off timing closure to layout tools

cadence

GLOBAL FOUNDRIES
FDXcelerator

ASIC Development

Verification Competence:

- **Tools**
  - Cadence (Incisive Verification Tool Chain)
  - Synopsys (VCS)
  - Mentor Graphics (Questa)

- **Methodology**
  - UVM Based Metric-Driven Verification (MDV)
    - Verification Management and Planning
    - UVM Verification Environments (Transaction Based & Self Checking)
    - Sequence Based Constrained Random Testing
    - Scoreboarding & Assertion Based Verification (ABV)
    - Functional Coverage Implementation
    - Web Based Metrics Analysis & Reporting
  - Verification Environment Add-Ons
    - UVM/OVM Based SystemVerilog Verification IP Library (DVLib)
    - SystemC Verification IP Library
    - ABV Library (PSL/SVA)
    - HW/SW Co-Verification
    - Behavioral Model Development (C++, SystemVerilog)
  - Infrastructure
    - Design Analysis and Verification Front-End Tool Set (SDA, SVI)
    - Web Based Regression Management Tool

Development Examples:

- Imaging ASIC, frontend development
  - Tensilica, 40 nm Toshiba
- Automotive dashboard controller IC, RTL/ DFT/ synthesis
  - Cortex R5, 55 nm Fujitsu
- Space application, backend development
  - redundant logic cells, 350 nm AMS
- ADAS ASIC development
  - low power high performance FDSOI technology, 22 nm GF FDSOI
- ASIC block level and toplevel UVM verification
  - high security mobile Cortex SC300, 40 nm TSMC
- Dual core processor chip backend development
  - high speed low power hierarchical layout, 65 nm TSMC

Dream Chip Technologies has developed ASICs using the following technologies:

- IFX 130 nm
- TSMC 130 nm, 65 nm, 45 nm, 40 nm, 28 nm
- SMIC 130 nm
- Global Foundries 130 nm, 28 nm, 22 nm FDSOI
- Toshiba 350 nm, 65 nm FFSA, 40 nm

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